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328356(28)

B. E. (Third Semester) Examination, Nov.-Dec. 2021

(New Scheme)

(Electronics & Telecommunication Engineering Branch)

DIGITAL LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) of each question is compulsory.*
Attempt any two parts from (b), (c) and (d).

Unit-I

1. (a) What is self complementary code?   2

    (b) Using Boolean algebra, prove that

(i) $AB + ABC + A\bar{B} = A$

(ii) $(B+A)(B+D)(A+C)(C+D) = BC + AD$

(iii) $1 + A' = 1$ 7

(c) Demonstrate by means of truth table the validity of the De Morgan's theorems (Both forms) for three variables.   7

(d) Write the short notes on Duality.   7

Unit-II

2. (a) Design Not Gate using Ex-OR Gate.   2

(b) Simplify the logic expression using K-map.

$$F(ABCD) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$$ 7

(c) Reduce the following expression using tabular method.

$$F(A, B, C, D) = \sum (0, 2, 3, 5, 8, 10, 11, 13)$$

and also design logic circuit using gates.   7

(d) Implement the following function using the don't-care conditions. Assume that both the normal and complement inputs are available.

$F = A'B'C' + AB'D + A'B'CD'$ with no more than two NOR gates.

$$d = ABC + AB'D'$$ 7

Unit-III

3. (a) Define Don't care Terms.   2

(b) Implement a full Adder using two half Adder and an OR gate.   7

(c) Design BCD-to-Excess-3 code converter.   7

(d) Implement full adder using Decoder.   7

Unit-IV

4. (a) Write two differences between Latch and Flip-flops.   2

(b) Draw the logic diagram of R-S flip-flop and explain its working to :   7

(i) Obtain the flip-flop characteristics table

(ii) Obtain characteristics equation

(iii) Obtain excitation table

(c) Design a counter with the following binary sequence :

0, 4, 2, 1, 6 and repeat. Use JK flip flops. 7

(d) Draw and descibe the working of a Serial-in-serial-out (SISO) shift register. Explain how a number can be shifted in and out from such register? 7

Unit-V

5. (a) What is Fan-IN and Fan-OUT? 2

(b) Compare the characteristics of DTL, TTL, RTL and ECL logic families. 7

(c) Draw the circuit diagram and explain the operation of 2 inputs TTL NAND gate. 7

(d) Draw and explain the basic CMOS inverter circuit. 7